Investigating Switching Transformers for Common Mode EMI Reduction to Remove Common Mode EMI Filters and Y-Capacitors in Flyback Converters

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***Abstract*— This paper investigated the common mode (CM) noise model for multiwinding switching transformers. Based on the proposed model, a Flyback transformer is investigated. A measurement technique is used to characterize and evaluate a switching transformer's CM noise performance. Only a signal generator and an oscilloscope are needed in this measurement technique. Because there is no any in-circuit tests are needed, the technique can help quickly design and evaluate transformers in mass testing. CM noise reduction techniques, including the balance capacitor technique, core shielding technique, balance winding technique, and winding design technique, are investigated based on the developed two-capacitance model and measurement technique without introducing extra power loss. The near-field capacitive coupling due to transformer magnetic cores is analyzed, and a core shielding technique is applied to reduce the coupling. Experimental results validated the proposed model and the developed CM noise reduction techniques. The Flyback converter can finally meet electromagnetic interference (EMI) standards without using CM EMI filters and Y-capacitors.**

***Index Terms*— AC/DC power adapter, balance, common mode (CM), electromagnetic interference (EMI), transformer, winding capacitance.**

I. Introduction

HIGH power density ac/dc power converters are popularly used in power adapters/chargers of portable electronics such as laptops, smart phones, and tablets. Electromagnetic interference (EMI) noise, such as common-mode (CM) noise leads to big EMI filters. To reduce EMI filter size, EMI such as CM EMI should be reduced. Various techniques have been developed to reduce CM noise for power converters [1], [2], [6], [7], [9], [11]–[13], [15]–[17].

AC/DC Flyback converters are popularly used in ac/dc power adapters/chargers because of their low cost, small size, and small number of components. Cochrane *et al.* [1], Kong *et al.* [2], Meng *et al.* [3], and Chu and Wang [9] analyzed the CM noise paths of Flyback converters: one path is from the drain of MOSFET to the earth ground, and the other path is from the noise source through the parasitic capacitances of the transformer to the secondary side and then to the earth ground, as shown in Fig. 1. In order to reduce the CM noise, CM inductors and Y-capacitors are usually used in an adapter.

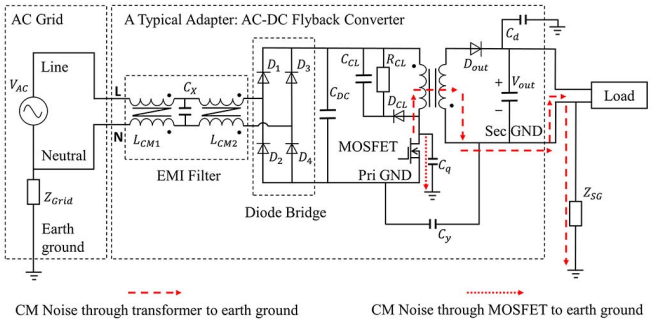

Fig. 1. CM current path including single-phase power line, a power adapter, a touchscreen enabled device, and a user.

If C_q represents the parasitic capacitance from MOSFET drain to MOSFET heatsink and then from the heatsink to the earth ground, the CM noise can flow from the MOSFET drain through C_q to the earth [1]. This CM noise can be eliminated by connecting the heatsink of MOSFET to primary ground (Pri GND) [4]. Based on the semiconductor structure of a diode, the major parasitic capacitance between a diode and its heatsink is C_d from its cathode to the heatsink. In Fig. 1, because the voltage potential of cathode is constant, the parasitic capacitance between the diode and the heatsink will not generate CM noise. The secondary heatsink can be grounded to secondary ground (Sec GND) so the parasitic capacitance between two heatsinks works as a Y-capacitor and it will not generate CM noise. In some applications, the MOSFET and the diode share the same heatsink. The heatsink can be equivalently grounded to Pri GND via a small capacitor; then, the CM noise can still be eliminated.

If the CM noise via heatsinks to the earth ground can be eliminated, the CM noise flowing through the parasitic winding capacitances between the transformer windings on

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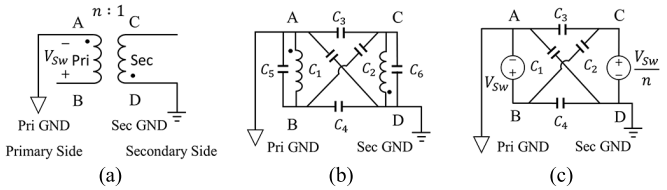

Fig. 2. Two-winding transformer (a) circuit, (b) six-capacitance model, and (c) four-capacitance CM model.

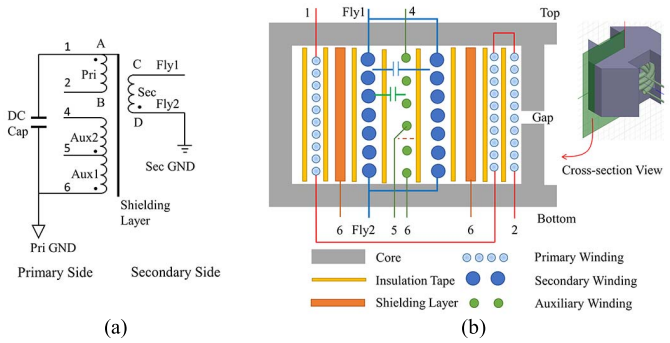

Fig. 3. Flyback transformer (a) circuit and (b) winding structure of one winding window.

the primary side and on the secondary side will be a major contributor to the CM noise. Therefore, a CM transformer winding capacitance model should be developed for CM noise analysis.

There are many studies discussing the modeling of parasitic capacitances of two-winding transformers with turn ratio n, as shown in Fig. 2. In Fig. 2, $V_{\rm Sw}$ is the switching voltage on the primary winding and $V_{\rm Sw}/n$ is the voltage on the secondary winding. From energy conservation point of view, as shown in Fig. 2(b), a two-winding transformer's parasitic capacitance can be modeled with six capacitances including four interwinding capacitances C_1–C_4 and two intrawinding capacitances C_5–C_6 [18]. However, when the nonlinear switching devices are substituted with noise voltage sources based on the substitution theory for CM noise analysis [9], [11], if a noise voltage source is equivalently in parallel with transformer windings, the two intrawinding capacitors can be removed. Therefore, the winding capacitance model can be reduced to four lumped capacitances, as shown in Fig. 2(b). Furthermore, based on the linear passive network theory, three independent capacitances are actually enough to characterize a linear two-port network. Based on this, Chu and Wang [9] used three independent capacitances to characterize a transformer's winding capacitance. Finally, in many power electronics applications, when the transformer windings are equivalently connected to at least one noise voltage sources, two capacitances are enough to characterize the interwinding parasitic capacitances of a two-winding transformer [10].

Flyback transformers typically use several auxiliary windings to achieve multiple outputs. Based on the conventional winding capacitance models of two-winding transformers in Fig. 2(c), it is difficult to analyze CM noise as there are too many capacitances. Theoretically, a transformer with n windings has $4 \cdot C_n^2 = 2n(n-1)$ parasitic capacitances. A more general and simpler model should be developed to analyze and reduce the CM noise flowing through the transformers. Moreover, if the CM performance of a transformer can be evaluated and balanced without doing any in-circuit tests, it will be very convenient for transformer design and evaluation in mass testing in industry applications as requested by the sponsor of this research. This paper will also introduce a technique to achieve this goal.

Balance techniques have been introduced in studies to reduce the CM noise due to transformer winding capacitances and they have two categories: 1) balancing transformers externally and 2) balancing transformers internally. In the first category, the most common technique is to add balance capacitors [3], [4] between the terminals of the windings across the primary and secondary sides. In the second category, the techniques include optimizing winding terminal connections [2], applying shielding layers [5], or using cancelation windings [6]. These techniques require extracting winding capacitance and implementing balance techniques. In this paper, an efficient balance design technique will be introduced to reduce the CM noise without using shielding layers between windings. The technique can achieve both CM noise reduction and small leakage inductance as using shielding layers increase the space between windings, therefore, lead to increased leakage inductance. (It will be addressed in detail in Section V.) Transformer core shielding technique will also be introduced to reduce the capacitive couplings due to the high permittivity of magnetic cores. Transformer prototypes were developed based on the developed techniques. Experiments were conducted to validate the developed techniques.

This paper is organized as follows. In Section II, a two-capacitance transformer winding capacitance model for multiwinding transformer is first introduced for CM noise analysis. Based on the model, a CM noise reduction methodology which includes several transformer CM noise reduction and design techniques is developed in Sections III–V. In Section III, a convenient technique to extract transformer's parasitic capacitance and evaluate transformer's CM noise performance without any in-circuit tests is introduced. An external capacitance balance technique is discussed. In Section IV, a transformer core shielding technique is analyzed to eliminate the capacitive coupling between the transformer core and heatsinks. In Section V, a design technique with an adjustable auxiliary winding is introduced to achieve CM noise balance and small leakage inductance without any in-circuit tests and complicated calculations. A transformer prototype is designed based on all the techniques above and the experimental results validated the developed techniques.

II. Two-Capacitance Transformer Model for Multiwinding Transformers

A. Two-Capacitance Model for Multiwinding Transformers

A Flyback transformer in Fig. 3(a) usually has several windings and may have shielding layers. Fig. 3(b) shows a

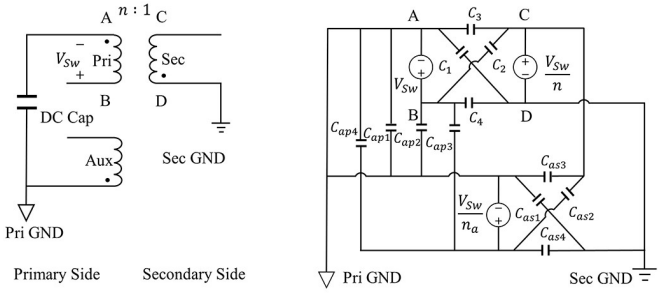

Fig. 4. Three-winding transformer (a) circuit and (b) its conventional CM model.

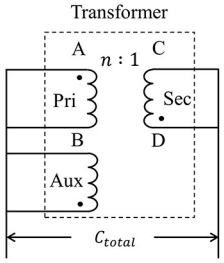

Fig. 5. Measure C_{Total} between the primary side and the secondary side.

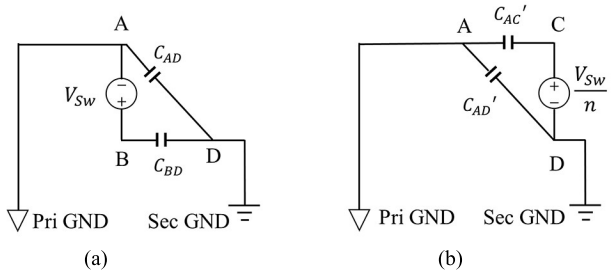

Fig. 6. Two-capacitance CM model of a multiwinding transformer. (a) Voltage source is on the primary side. (b) Voltage source is on the secondary side.

transformer using RM cores. Its typical winding structure in a cross-sectional view is shown in Fig. 3(b). The transformer uses interleaved windings to reduce the leakage inductance so as to reduce parasitic ringings during switching transitions, to reduce semiconductor device voltage stress and to improve converter efficiency. There are also two auxiliary windings used to supply power to the control chip. Two shielding layers are connected to the primary to bypass the CM noise flowing from the primary side. The air gap of the core is on the center leg.

If the winding turns in a winding layer are sparse (for example, an auxiliary winding layer), the parasitic capacitance between the two layers adjacent to this layer cannot be ignored [for example, the capacitance between two secondary winding layers in Fig. 3(b)]. The theoretical capacitance calculation would be difficult, and it is also very difficult to directly measure these capacitances. Furthermore, the capacitances between windings and the core cannot be ignored unless they are much smaller than those between two windings and they are complicated to calculate [23] or measure [5] too. A simplified model and a convenient technique to extract the parasitic capacitance are demanded by industry sponsors.

In the transformer's conventional CM noise model shown in Fig. 2(c), the winding capacitances C_1, C_2, C_3, and C_4 represent the effects of the capacitances directly between two windings and those between the two windings through the core.

When the conventional modeling technique in Fig. 2(b) is applied to a three-winding transformer in Fig. 4(a), the CM model is very complicated with 12 capacitances, as shown in Fig. 4(b). The turn ratios between the primary and the secondary and between the primary and the auxiliary are n and n_a, respectively. Since the impedance of the dc bus capacitor is very small in the concerned frequency range, primary and auxiliary winding are shorted by the dc capacitor. So, terminal A of the primary winding is shorted to primary GND in Fig. 4(b).

In this paper, a two-capacitance model will be developed to characterize the winding capacitance of transformers with multiple windings. The model in Fig. 4(b) can be reduced by removing capacitances C_{ap1}–C_{ap4} because they are fully located on primary side and they do not contribute to CM noise [2]. The same conclusion can be drawn based on the circuit analysis in Fig. 4: C_{ap1}–C_{ap4} are either parallel with voltage source or shorted.

The CM noise source V_{Eq} and impedance Z_{Eq} of the Thevenin equivalence between primary GND and secondary GND are given by (1)–(3), respectively.$C_{\text{Total}}$is the total capacitance between all the windings on the primary side and all the windings on the secondary side. It can be measured using an impedance analyzer as shown in Fig. 5 and derived using (1)–(6), as shown at the bottom of the next page.

In (1)–(3), the Thevenin equivalent voltage source V_{Eq} between the Pri GND and Sec GND is equivalently the output of a voltage divider composed of two series capacitances across the voltage source V_{SW}. Of these two capacitances, one capacitance is connected between transformer terminal A (one terminal of V_{Sw}) and D (Sec GND) and the other is connected between terminal B (another terminal of V_{Sw}) and D (Sec GND). These two lumped capacitances are, therefore, C_{BD} and C_{AD}, and their total is equal to C_{Total} as shown in (4)–(6) and Fig. 6.

Mathematically, C_{BD} and C_{AD} could be either positive or negative depending on winding structure and turns ratios. Based on (2), (5), and (6), only two independent capacitances and one voltage source are enough to describe the CM behavior of a multiwinding transformer. The model shown in Fig. 6(a) can be used to characterize transformer's CM model. Fig. 6(b) shows another model based on the secondary voltage V_{Sw}/n.

In Fig. 6(b), C'_{AC}, C'_{AD}, and V'_{Eq} are

$$C'_{\text{AC}} = n(C_2 + C_4) + \frac{n}{n_a}(C_{\text{as2}} + C_{\text{as4}}) - (C_2 + C_3 + C_{\text{as2}} + C_{\text{as3}}) \quad (7)$$

$$C'_{\text{AD}} = C_{\text{Total}} - C'_{AC} \quad (8)$$

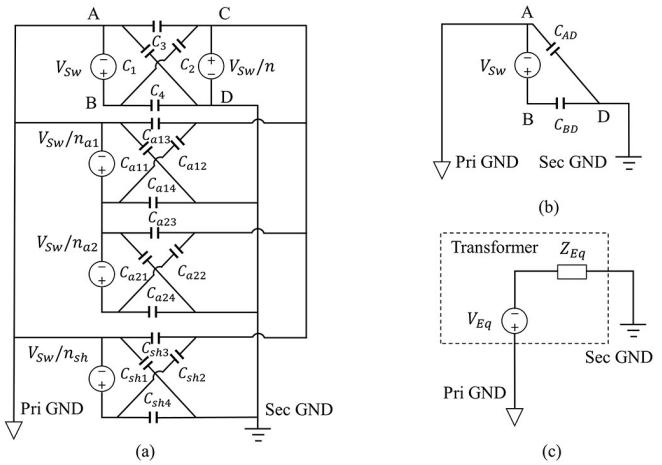

Fig. 7. Lumped CM parasitic capacitance model for a Flyback transformer. (a) Conventional model. (b) Thevenin equivalence. (c) Two-capacitance model.

$$V'_{\mathrm{Eq}} = \frac{C'_{AC}}{C'_{AC} + C'_{\mathrm{AD}}} \frac{V_{\mathrm{SW}}}{n}. \tag{9}$$

Similarly, the voltage source can be normalized to the auxiliary winding side for the third CM model. Based on a similar derivation to the above, the CM model of the Flyback transformer in Fig. 3 with a primary, a secondary, two series auxiliary windings, and one shielding layer can be developed in Fig. 7. The turn ratios of primary to secondary, primary to auxiliary 1, primary to auxiliary 2, and primary to shielding layers are n, n_{a1}, n_{a2}, and n_{sh}, respectively. The transformer is first modeled with the conventional technique in Fig. 7(a). The four parasitic capacitances between any two windings are shown and labeled in Fig. 7(a) correspondingly. Equations (10) and (11) are Thevenin CM equivalent voltage source V_{Eq} and impedance Z_{Eq} between Pri GND and Sec GND. C_{AD} and C_{BD} in the final two-capacitance CM model in Fig. 7(c) can be directly solved based on Fig. 7(a) and (b) and the results are shown in (12) and (13)

$$V_{\mathrm{Eq}} = \frac{C_{\mathrm{BD}}}{C_{\mathrm{BD}} + C_{\mathrm{AD}}} \cdot V_{\mathrm{SW}} = \frac{C_{\mathrm{BD}}}{C_{\mathrm{Total}}} \cdot V_{\mathrm{SW}} \tag{10}$$

$$Z_{\mathrm{Eq}} = \frac{1}{j\omega(C_{\mathrm{BD}} + C_{\mathrm{AD}})} = \frac{1}{j\omega C_{\mathrm{Total}}} \tag{11}$$

$$C_{\mathrm{BD}} = \left[\left(1 - \frac{1}{n}\right) \cdot C_2 + C_4 - \frac{1}{n} \cdot C_3\right] + \left[\left(\frac{1}{n_{a1}} - \frac{1}{n}\right) \cdot C_{a12} + \frac{1}{n_{a1}} \cdot C_{a14} - \frac{1}{n} \cdot C_{a13}\right] + \left[\frac{1}{n_{a1}} \cdot C_{a21} + \left(\frac{1}{n_{a1}} + \frac{1}{n_{a2}} - \frac{1}{n}\right) \cdot C_{a22} + \left(\frac{1}{n_{a1}} - \frac{1}{n}\right) \cdot C_{a23} + \left(\frac{1}{n_{a1}} + \frac{1}{n_{a2}}\right) \cdot C_{a24}\right] + \left[\left(\frac{1}{n_{\mathrm{sh}}} - \frac{1}{n}\right) \cdot C_{\mathrm{sh2}} + \frac{1}{n_{\mathrm{sh}}} \cdot C_{\mathrm{sh4}} - \frac{1}{n} \cdot C_{\mathrm{sh3}}\right] \tag{12}$$

$$C_{\mathrm{AD}} = C_{\mathrm{Total}} - C_{\mathrm{BD}}. \tag{13}$$

The model in Fig. 7(b) and (c) was derived based on two conditions.

1) The effect of leakage inductance of a transformer is insignificant, so the transformer's winding voltages are linearly dependent. This means the impedance of the leakage inductance of the transformer should be much smaller than the impedance of the total parasitic winding capacitance C_{total} between the primary and secondary windings.
2) One of the transformer windings is connected to an independent equivalent voltage source as the V_{SW} shown in Fig. 7(a). As long as the two conditions are satisfied, the model is valid. For example, the modeling technique can be applied to transformers with multiwindings on the secondary side or to other converter topologies. An LLC converter and a push–pull converter with more than one secondary windings will be discussed in Section III-C.

When the two conditions above cannot be met, the model will be inaccurate. This happens when frequency increases and the impedance of leakage inductance L_{lk} becomes higher than that of C_{total}. The boundary frequency below which the model is considered valid can be approximately given by $1/(2\pi(L_{lk} \cdot C_{\mathrm{total}})^{1/2})$. Also, above this frequency, the CM noise spikes caused by the resonance between the leakage inductance and parasitic capacitance of MOSFET [21] should not be analyzed with this model.

B. Common Mode Noise Model for a Flyback Converter

An actual CM noise measurement setup for a commercial ac/dc adapter is shown in Fig. 8. The transformer is the same one as in Fig. 3.

In this commercial Flyback converter, the primary heatsink is connected to the Pri GND and the secondary diode heatsink is connected to Sec GND. C_{q1} is the drain to heatsink parasitic

$$V_{\mathrm{Eq}} = \frac{(C_2 + C_4) + (C_{\mathrm{as2}} + C_{\mathrm{as4}})/n_a - (C_2 + \mathrm{C}_3 + C_{\mathrm{as2}} + C_{\mathrm{as3}})/n}{C_{\mathrm{Total}}} \cdot V_{\mathrm{SW}} \tag{1}$$

$$Z_{\mathrm{Eq}} = \frac{1}{j\omega C_{\mathrm{Total}}} \tag{2}$$

$$C_{\mathrm{Total}} = (C_1 + C_2 + C_3 + C_4) + (C_{\mathrm{as1}} + C_{\mathrm{as2}} + C_{\mathrm{as3}} + C_{\mathrm{as4}}) \tag{3}$$

$$C_{\mathrm{BD}} = (C_2 + C_4) + \frac{1}{n_a}(C_{\mathrm{as2}} + C_{\mathrm{as4}}) - \frac{1}{n}(C_2 + C_3 + C_{\mathrm{as2}} + C_{\mathrm{as3}}) \tag{4}$$

$$C_{\mathrm{AD}} = C_{\mathrm{Total}} - C_{\mathrm{BD}} \tag{5}$$

$$V_{\mathrm{Eq}} = \frac{C_{\mathrm{BD}}}{C_{\mathrm{AD}} + C_{\mathrm{BD}}} V_{\mathrm{SW}} \tag{6}$$

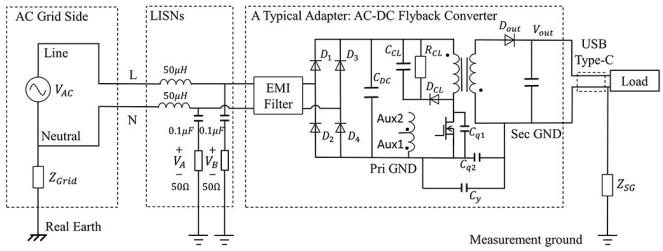

Fig. 8. CM noise measurement setup for a Flyback ac/dc adapter.

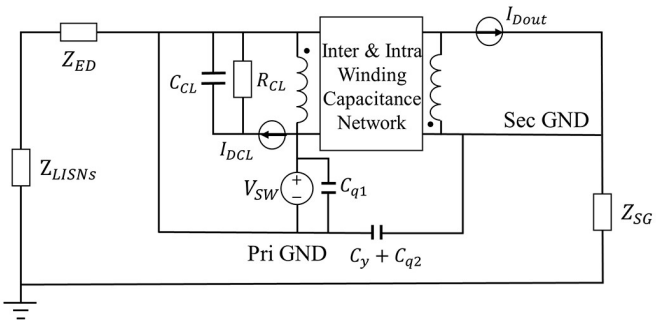

Fig. 9. Circuit topology of a Flyback converter with the substitution theory applied.

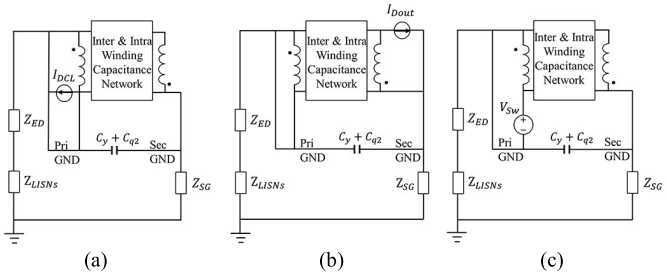

Fig. 10. CM models of a Flyback converter with the superposition theory applied. Effect of (a) I_{DCL}, (b) I_{Dout}, and (c) V_{Sw}.

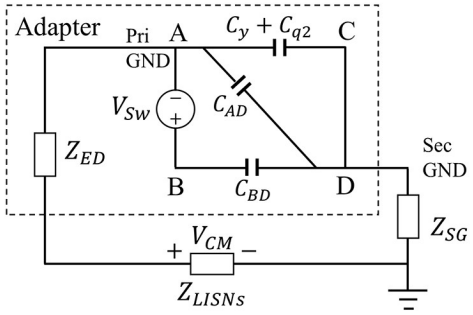

Fig. 11. Final CM model of a Flyback converter.

capacitance. There is a metal shielding box enclosing the whole Flyback adapter and it is connected to the Sec GND. Because of this, there is parasitic capacitance between primary heatsink and the metal shielding box which is connected to Sec GND; and parasitic capacitance between the primary heatsink and the secondary heatsink. These two parasitic capacitances are in parallel and the total is C_{q2} in Fig. 8. There is no parasitic capacitance from heatsink to the measurement ground due to the metal shielding box. C_y is the Y-capacitor connected between Pri GND and Sec GND. C_{q2} is, therefore, in parallel with C_y. Because the metal shielding box has parasitic capacitance to the measurement ground and the dc output including both V_{out} line and Sec GND is connected to the metal shielding box, there is a parasitic capacitance between the dc output and the measurement ground. Z_{SG} represents this impedance. In Fig. 8, when high-frequency CM noise is analyzed, the dc capacitor can be treated as short circuit, and the LISNs can be characterized as a 25-Ω resistor. When a pair of diodes in the diode bridge conducts currents, the diode bridge impedance is very small so the CM noise is the highest. The CM EMI filter of the adapter under investigation has a CM inductor only. The CM inductor's impedance is Z_{ED}. The transformer, including primary, secondary, and auxiliary windings, is represented with a block in Fig. 9 and it will be replaced with a two-capacitance model later. Based on the substitution theorem, all the voltages and currents of a network will not change if the nonlinear switching devices in the network are replaced with voltage or current sources which have the exact the same voltage or current waveforms as the original components to be replaced [9], [11]. The CM noise model of the Flyback converter can, therefore, be represented by Fig. 9.

Based on the techniques developed in [9] and [11], the MOSFET in Fig. 8 can be substituted with a voltage source V_{SW} which has the same voltage waveforms as the drain to source voltage. The snubber diode is replaced with a current source I_{DCL} which has the same current waveforms as the diode current and the rectifying diode on the secondary side is replaced with a current source I_{Dout} which has the same current waveforms as the diode current. Based on the network theory, the components in parallel with voltage sources or in series with current sources can be removed since they do not contribute to the voltages or currents of the network. Because of this, in Fig. 9, C_{CL}, R_{CL}, and C_{q1} can be removed. Based on the superposition theory, the effects of I_{DCL}, I_{Dout}, and V_{Sw} can be analyzed in Fig. 10(a)–(c) separately.

In Fig. 10(a) and (b), it is obvious that I_{DCL} and I_{Dout} do not generate CM noise as they are shorted. Only V_{Sw} in Fig. 10(c) generates CM noise. CM current flows through the transformer parasitic capacitance to the secondary side, and then flows back to the input of converter through Z_{SG}, Z_{LISNs}, and Z_{ED}.

If the transformer and its parasitic capacitance are replaced with a two-capacitance model developed in Fig. 7(c), the final CM model can be shown in Fig. 11. Based on Fig. 11, the CM noise voltage on LISNs is

$$V_{\mathrm{CM}} = \frac{Z_{\mathrm{LISN}}}{j\omega(C_{\mathrm{Total}} + C_y + C_{q2}) + Z_{\mathrm{LISN}} + Z_{\mathrm{ED}} + Z_{\mathrm{SG}}} \cdot \frac{C_{\mathrm{BD}}}{C_{\mathrm{Total}} + C_y + C_{q2}} \cdot V_{\mathrm{SW}}. \quad (14)$$

The techniques can be developed to reduce CM noise based on Fig. 11 and (14). For example, C_{BD} should be reduced as much as possible by improving transformer winding structure or by adding external capacitor across primary and secondary windings. Using a large Y-cap C_y also helps to reduce CM noise. However, it increases the total capacitance between

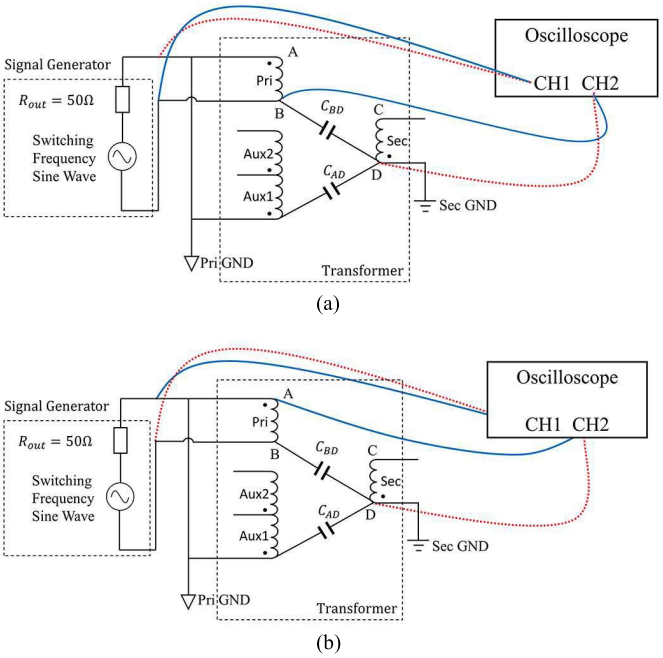

Fig. 12. Extract parasitic capacitance. Extract (a) C_{AD} and (b) C_{BD}.

primary and secondary side, which will in turn increase the leakage current from the primary side to the secondary side and might cause safety concerns [19]; thus, it may not be desired. Using a big CM inductor to increase Z_{ED} also helps to reduce CM noise but it will increase the size and the cost of the converter; therefore, it may not be a perfect solution either. Because of these, the best solution is to reduce C_{BD} of the transformer. In this paper, it will be shown that the CM noise of a Flyback adapter can meet the EMI standard with the proposed technique without using any CM chokes ($Z_{ED} = 0$) and Y-caps.

III. Technique of Evaluating Transformer's CM Noise Performance

A. Technique to Extract Parasitic Capacitance and Evaluate Transformer's CM Noise Performance

In (3) and (5), the total capacitance C_{Total} is the sum of the C_{BD} and C_{AD} and it can be directly measured similar to that shown in Fig. 5. To extract C_{BD} and C_{AD}, a sinusoidal signal at switching frequency from a signal generator is first added between terminals A and B in Fig. 12. Since both the terminal A of the primary winding and one terminal of auxiliary windings are connected to input dc bus, the two terminals are equivalently connected to each other through a dc bus capacitor on primary side within the concerned frequency range. The measurement setup in Fig. 12 is to emulate this actual condition. Similarly, if a transformer has more than one secondary windings, the winding terminals which are efficiently shorted via dc capacitors within the concerned frequency range should be connected in the measurement.

In the second step, an oscilloscope is used to measure both the signal V_{AB} between terminals A and B, and the signal V_{DB} between terminals D and B as shown in Fig. 12(a). In the third step, an oscilloscope is used to measure V_{BA} between terminals B and A, and V_{DA} between terminals D and A as shown in Fig. 12(b). Based on the ratio of V_{DB}/V_{AB} and V_{DA}/V_{BA}, C_{BD} and C_{AD} can be calculated based on (15) and (16). In (15) and (16), C_{probe} is oscilloscope probe's input capacitance which is in parallel with the C_{BD} or C_{AD}. C_{probe} can be obtained from datasheet or measured via an impedance analyzer. The probe's input resistance can be ignored as it is much higher than the impedances of capacitances at the signal frequency

$$\frac{V_{DB}}{V_{AB}} = \frac{C_{AD}}{C_{total} + C_{probe}} \tag{15}$$

$$\frac{V_{DA}}{V_{BA}} = \frac{C_{BD}}{C_{total} + C_{probe}}. \tag{16}$$

It should be pointed that as shown in (14), if C_{BD} equals to zero, the CM noise flowing through the transformer is zero. In other words, if the measured V_{DA} in (16) is zero, the CM noise flowing through the transformer will be zero. This would be a very convenient technique to check if a transformer is well balanced.

Since C_{BD} and C_{AD} can be measured, respectively, if C_{Total} equals to the sum of C_{AD} and C_{BD}, the measurement results are validated. The precision of the method will be discussed in Section III-B based on experimental data.

Since C_{AD} or C_{BD} are just equivalent capacitances, the value of C_{AD} and C_{BD} can be positive or negative. From (15) and (16), if V_{DB} or V_{DA} is in phase of V_{AB} or V_{BA}, C_{AD} or C_{BD} is positive. If V_{DB} or V_{DA} is out phase of V_{AB} or V_{BA}, C_{AD} or C_{BD} is negative.

The advantages of the proposed parasitic capacitance extraction technique are as follows.

1) A transformer's CM performance can be evaluated with a signal generator and an oscilloscope without any in-circuit tests. Therefore, it is convenient to test the transformer's CM performance during design and manufacturing process.
2) The two capacitances can be easily extracted without the knowledge of transformer winding structures.
3) Unlike many studies, in which transformer's winding structure must be investigated, the proposed measurement technique can efficiently identify the unbalanced capacitance.

B. CM Noise Reduction With a Balance Capacitor

A commercial 45 W, 120-V ac/20-V dc, Flyback converter with a multiwinding transformer as shown in Fig. 3(b) is used to verify the developed model. The load is a 15-Ω resistor. Both CM EMI filter and Y-cap are removed. The number of turns of primary, secondary, two auxiliary windings, and shielding layer is 40, 8, 8, 16, and 1, respectively. Therefore, n, n_{a1}, n_{a2}, and n_{sh} in (12) are equal to 5, 5, 2.5, and 40, respectively. C_{Total} of the transformer is measured as 105 pF. The capacitance of oscilloscope voltage probe is 15 pF. Fig. 13(a) shows the measured voltage waveforms of V_{BA} and V_{DA}. Since V_{DA} is in phase of V_{BA}, C_{BD} is positive. C_{BD} is calculated from (16) as 9.5 pF. Similarly, C_{AD} is derived

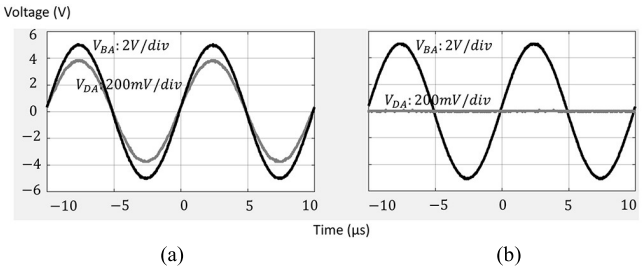

Fig. 13. Waveforms of V_{BA} and V_{DA} (a) before balance and (b) after adding a 47-pF balance capacitor C_{ext} based on (12) and (17).

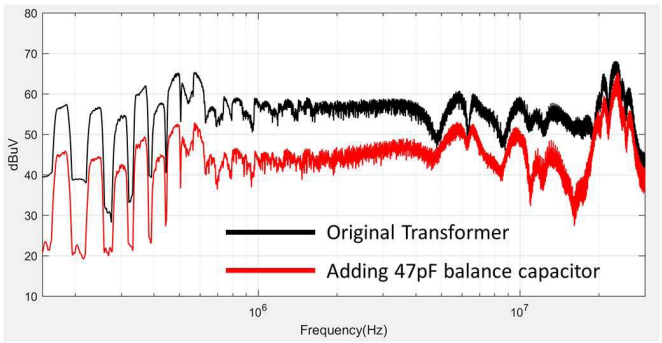

Fig. 14. Measured CM noise of the power adapter before and after adding a balance capacitor.

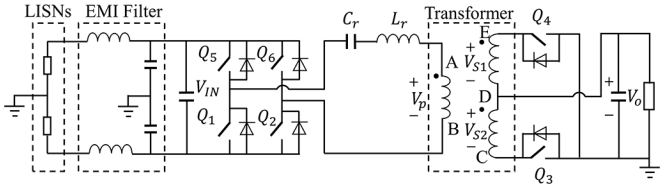

Fig. 15. Circuit of a full-bridge LLC resonant converter.

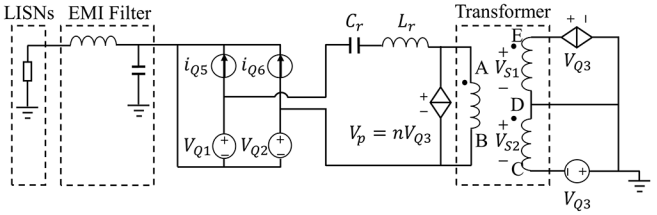

Fig. 16. Circuit of a full-bridge LLC resonant converter with the substitution theory applied.

from (15) by measuring V_{AB} and V_{DB} and it is found as 91 pF. Since the sum of C_{AD} and C_{BD} is very close to C_{Total} (the error is 4.3%), the measured results are verified.

Although many studies discussed the technique of adding a balance capacitor to reduce CM noise, this paper proposes a simple but efficient technique to determine balance capacitor's value and position. In (12), each capacitance has a coefficient which could be either positive or negative mostly depending on the turn ratios. To balance a positive/negative C_{BD}, increasing the sum of negative/positive terms by paralleling an external capacitor to any capacitance with negative/positive coefficient can cancel the sum of all positive/negative terms in C_{BD}. The capacitance of this external capacitor should be equal to the absolute value of the product of C_{BD} and the inverse of the coefficient of the capacitance with which the external capacitor to be paralleled with. For example, a positive C_{BD} can be balanced to zero by paralleling a capacitor equal to nC_{BD} with C_3, C_{a13}, or C_{sh3}, across terminals A and C between the secondary and primary sides because their coefficient is $1/n$. For the transformer under investigation, $nC_{BD} = 47$ pF. As another example, if C_{BD} is negative, based on (12), an external balance capacitor equal to $1 \times |C_{BD}|$ can be paralleled with C_4 across terminals B and D because C_4's coefficient is 1. In summary, the external balance capacitor should have a capacitance C_{ext} meeting condition

$$C_{ext} = \left| \frac{1}{k} C_{BD} \right| \tag{17}$$

where k is the coefficient of the capacitance with which the external capacitor to be paralleled with in (12). k must have a polarity reverse to that of C_{BD}.

The measured V_{DA} after C_{BD} is balanced which is shown in Fig. 13(b). It is almost zero which indicates the transformer is well balanced. The EMI measurement was conducted on a Flyback converter as shown in Fig. 1 but with the EMI filter removed. The comparison of the measured CM noise before and after balance is shown in Fig. 14. The external balance capacitor reduced the CM EMI noise by up to 10 dB from 150 kHz to 18 MHz.

The balance capacitor increases the total capacitances between the primary and the secondary side. It therefore increases 50-/60-Hz leakage current from primary to secondary and results in safety concerns. Under some faulty conditions, the balance capacitor could be shorted, so the primary and secondary will lose galvanic isolation. Therefore, in some cases, it may not be desired to use external balance capacitor. A better technique will be discussed in Section V.

C. Extend the Technique to Other Topologies

The transformer model derived in Section II is valid if the two conditions defined in Section II-A are satisfied. The transformer model can be applied to many power converters such as LLC, forward and push–pull converters. Figs. 15–17 show the example of a full-bridge LLC resonant converter.

In Fig. 15, based on the substitution theory, nonlinear switches can be replaced with voltage or current sources for EMI analysis [9], [11]. The CM noise model can, therefore, be derived in Fig. 16. Similar to the analysis in Section II, i_{Q5} and i_{Q6} do not contribute to CM noise and the final CM model is derived in Fig. 17. Based on full-bridge LLC converter's characteristics, $V_{Q1} = -V_{Q2}$. Since the switching frequency is very close to the resonant frequency, the total voltage drop on L_r and C_r is close to zero, so $V_p \approx V_{Q1} - V_{Q2}$. The Thevenin CM equivalent voltage source V_{Eq} and impedance Z_{Eq} between Pri GND and Sec GND are

$$V_{Eq} = \frac{C_{BD} - C_{AD}}{C_{BD} + C_{AD}} \cdot V_{Q2} \tag{18}$$

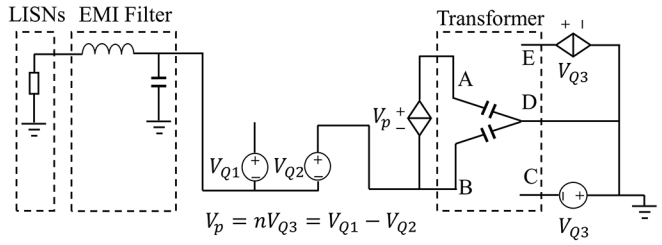

Fig. 17. Final CM noise model of a full-bridge LLC resonant converter.

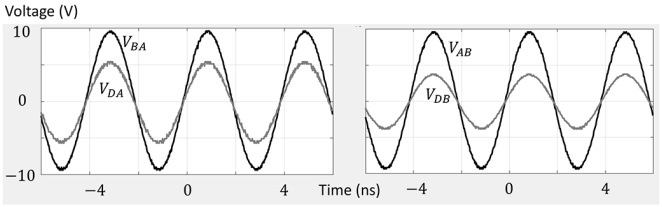

Fig. 18. Measured voltage waveforms to extract C_{AD} and C_{BD}.

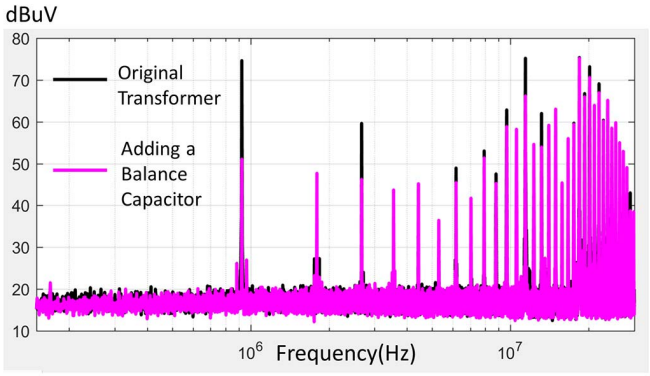

Fig. 19. Measured CM noise of the full-bridge LLC resonant converter without and with the balance capacitor.

$$Z_{\text{Eq}} = \frac{1}{j\omega(C_{\text{BD}} + C_{\text{AD}})} = \frac{1}{j\omega C_{\text{Total}}}. \tag{19}$$

Based on (18), the condition for CM noise balance is, therefore, $C_{\text{AD}} = C_{\text{BD}}$. The value of C_{AD} and C_{BD} can be measured similar to those in Section III-A. C_{Total} is measured as 4.2 nF. As shown in Fig. 18, C_{BD} can be extracted with V_{BA} and V_{DA}; C_{AD} can be extracted with V_{AB} and V_{DB}. Based on (15) and (16), the values of C_{AD} and C_{BD} are 1.68 and 2.52 nF, respectively. In this case, C_{probe} can be ignored since it is much smaller than C_{AD} and C_{BD}. By connecting a 0.84-nF balance capacitor between A and D in Fig. 17, the balance condition is achieved. Fig. 19 shows the measured CM noise and it verifies the model and the CM reduction technique in this section.

Figs. 20 and 21 show the circuit topologies and final CM models of forward and push–pull converters.

IV. CM Noise Reduction by Reducing the Transformer Capacitive Couplings

It is found that in some commercial products, the capacitive couplings exist between transformer windings and heatsinks,

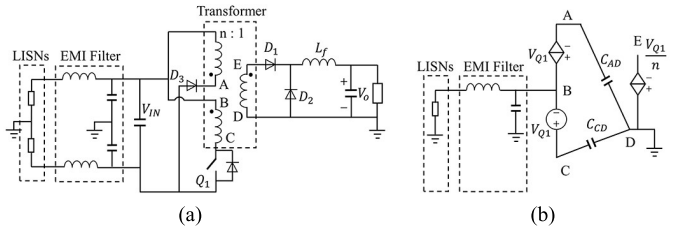

Fig. 20. CM noise model of a forward converter (a) topology and (b) final CM model.

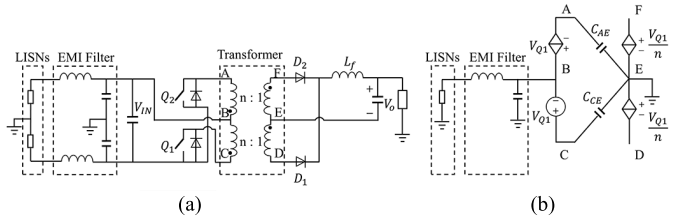

Fig. 21. CM noise model of a push–pull converter (a) topology and (b) final CM model.

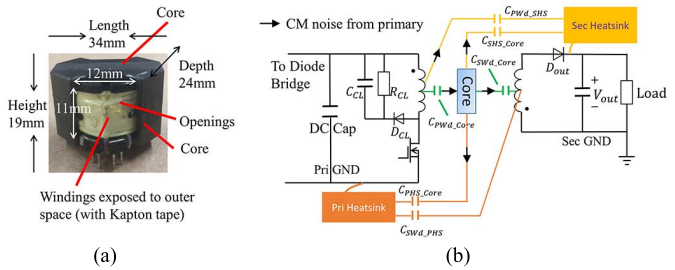

Fig. 22. Capacitive coupling due to a transformer core. (a) Transformer prototype with an RM core. (b) Capacitive couplings due to the magnetic core.

and between transformer magnetic cores and the heatsinks. They play an important role on CM EMI because the couplings cause CM noise flow between the primary and secondary sides. This is especially important when the transformer is physically close to the heatsinks of the primary and the secondary sides. The capacitive coupling between transformer windings and heatsinks is due to the fact that part of the transformer windings on the two openings of the transformer cores are exposed to the free space, as shown in Fig. 22(a). The transformer winding has high $\mathrm{d}v/\mathrm{d}t$, so any capacitive couplings between the transformer windings and other circuits can leads to induced displacement EMI currents. The capacitive coupling between transformer magnetic cores and the heatsinks is due to the fact that the magnetic cores such as ferrite cores have not only high permeability but also high permittivity, so they have a low impedance to electrical field. The stray near electric field generated by the high $\mathrm{d}v/\mathrm{d}t$ nodes in the circuit can be easily coupled through the transformer cores to other components nearby. Fig. 22(b) shows the capacitive couplings among the transformer core, heatsinks, and transformer windings. In Fig. 22(b), since the transformer is the primary research object, the diode bridge, EMI filter, and ac source are omitted to highlight the transformer and save space.

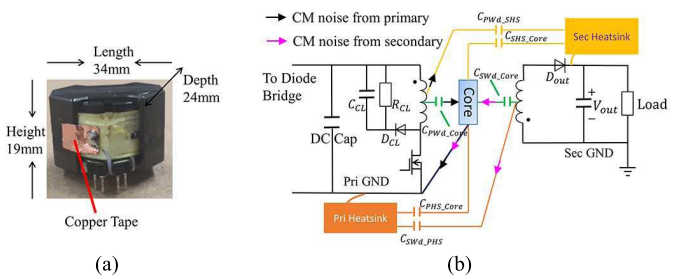

Fig. 23. Grounding the magnetic core can eliminate part of CM noise due to transformer capacitive couplings. (a) Prototype with core grounded and (b) CM noise paths.

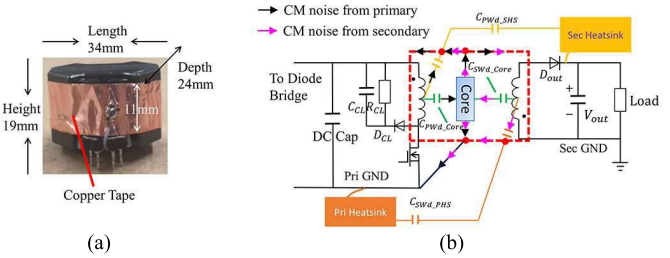

Fig. 24. Grounding the magnetic core and shielding the windings can eliminate most of CM noise. (a) Prototype with core grounded and winding shielded and (b) CM noise paths.

In Fig. 22(b), there are parasitic capacitance $C_{\text{PHS\_Core}}$ between the heatsink, which is connected to the Pri GND, of MOSFET and the core, $C_{\text{PWd\_Core}}$ between the primary winding and the core, $C_{\text{SWd\_Core}}$ between the secondary winding and the core, and $C_{\text{SHS\_Core}}$ between the heatsink, which is connected to the Sec GND, of the diode and the core. There are also parasitic capacitance $C_{\text{PWd\_SHS}}$ between the exposed primary winding part and the heatsink of the diode, $C_{\text{SWd\_PHS}}$ between the exposed secondary winding part and the heatsink of MOSFET. The parasitic capacitances between the exposed primary winding part and the heatsink of MOSFET, between the exposed secondary winding part and the heatsink of diode are ignored as they do not generate CM noise. The CM noise can flow between primary side and secondary sides through these parasitic capacitances because of the *dv/dt* across these parasitic capacitances. Fig. 22(b) shows the CM noise flowing from the primary winding to the heatsink of the diode, from the primary winding to the core and then to the secondary winding, to the heatsink of the diode or to the heatsink of the MOSFET. The CM noise can also flow from the secondary winding to the primary side similarly. The auxiliary winding on primary side has a similar story to the primary winding and will not be discussed in detail here.

Because the CM noise due to the parasitic capacitance between transformer windings has been greatly reduced with the balance technique in Section III, the CM noise due to the capacitive couplings in Fig. 22 will become significant.

One of the solutions is to ground the transformer core to the Pri GND, as shown in Fig. 23. A small copper foil is attached to the core and connected to the primary dc bus, as shown in Fig. 23(a) and (b). The CM noise flowing from primary windings to the core can be shorted back to the primary side, as shown in Fig. 23(b). However, the CM noise can still flow from the primary winding to the heatsink of the diode and the CM noise generated by the secondary winding can still flow to the primary side.

A better solution is to shield both transformer windings and the core using a copper foil connected to the dc bus on primary side, as shown in Fig. 24. All CM noise flowing from primary winding can be shorted back to the primary side through the shielding. However, the CM noise generated by the secondary winding can still flow to the primary side, as shown in Fig. 24(b). The introduction of shielding may slightly change the balance condition because of the parasitic

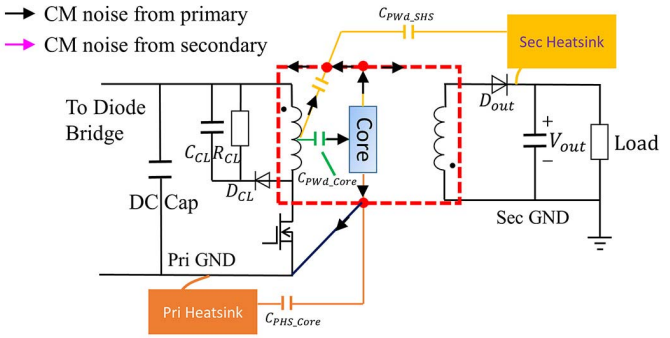

Fig. 25. Further optimize winding structure can eliminate all of CM noise.

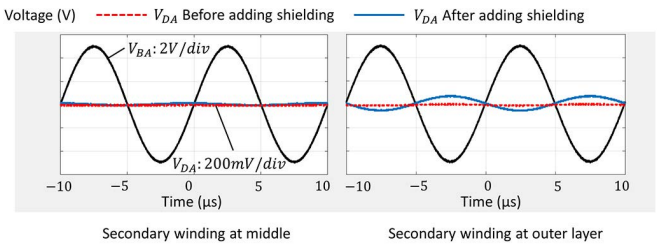

Fig. 26. Balance comparison before and after adding core shielding with different secondary winding positions.

capacitance between the shielding and windings. Parasitic capacitance can be re-extracted to achieve a new balance with the technique discussed in Section III.

An alternative is to adjust the secondary winding to be in the middle of the windings after applying the second solution above. As a result, the parasitic capacitance between the secondary winding and the core is very small, and the parasitic capacitance between the secondary winding and the heatsink of the MOSFET is also very small so they can be ignored, as shown in Fig. 25. With this solution, a rebalance is not required. The comparison of the balance before and after adding the core shielding is shown in Fig. 26. It is shown that after adding the shielding, when the secondary winding is in the middle, the balance condition does not change. On the other hand, when the secondary winding is at outer layer, the balance condition is slightly changed.

In order to verify the developed theory and technique, five measured CM noise curves are compared in Fig. 27: CM

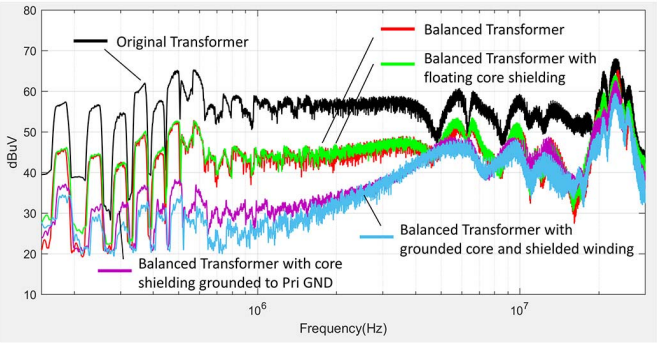

Fig. 27. Comparison of the measured CM noise with and without core copper shielding for the transformer.

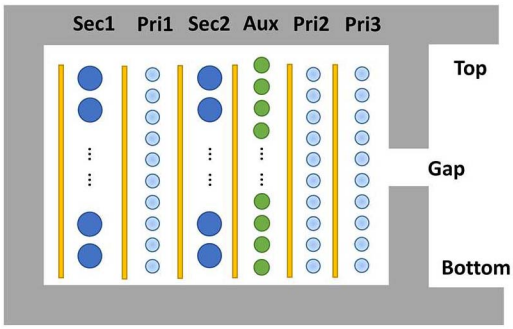

Fig. 28. Step 1: apply interleaving winding structure to reduce the leakage inductance.

noise without any measures taken, CM noise with a balanced transformer, CM noise with a balanced transformer and a floating core copper shielding, CM noise with a balanced transformer and a grounded core shielding, and CM noise with a balanced transformer, a grounded core and winding shielding. It is obvious that a floating copper shielding cannot shield capacitive coupling [14]; therefore, the CM noise is not reduced. By connecting the copper shielding to Pri GND, the CM noise is reduced. And by shielding the winding, the noise is further reduced and the CM noise can be reduced by 35 dB. The measurement results verified the analysis above.

Since the copper shielding is attached to the core, it also works as a heatsink of the transformer. Also, if the airgap of the core is at the center leg, the core shielding will not cause additional eddy current power loss. The analysis will be conducted in Section V.

V. Transformer Design With Small Leakage Inductance and CM Noise Balance

A. Flyback Transformer With Small Leakage Inductance and CM Noise Balance

The leakage inductance of the transformer causes high-frequency ringing with the intrinsic capacitance of the MOSFET during turning-OFF process [21], which results in extra power loss and high frequency spikes in EMI spectrum. Winding interleaving is a common technique to reduce the leakage inductance. Although a Flyback transformer is more like a coupled inductor rather than a transformer because the currents will not flow in primary and secondary windings at the same time, as discussed in [12], with interleaving technique, leakage inductance will be reduced.

Unfortunately, interleaving may not be good for CM noise reduction as it may increase the parasitic capacitances between windings. In order to solve this problem, shielding layers were added between the primary and secondary windings in commercial products. For example, the transformer in Fig. 3(b) has two shielding layers connected to a primary node with constant voltage potential to reduce CM noise. However, this increases the leakage inductance between two windings as it increases the distance between windings. The shielding layers also increase the cost and size of the transformer. Therefore, a better technique needs to be developed.

An alternative technique is to add an auxiliary winding on primary side and make it adjacent to the secondary windings. The voltage on the auxiliary winding can be adjusted to achieve CM noise balance by adjusting its number of turns. This technique was introduced in [13], but there is no discussion on its design and the analysis of additional power loss due to this winding.

In this section, a design technique is introduced to achieve CM balance and reduced leakage inductance without any in-circuit tests and complicated calculations. The power loss due to this auxiliary winding is also analyzed.

B. Flyback Transformer Design

The Flyback transformer in Fig. 3(b) is to be redesigned to achieve both CM balance and small leakage inductance.

Windings interleaving technique is applied in the first step to reduce leakage inductance. A winding structure of Sec1-Pri1-Sec2-Aux-Pri2-Pri3 is employed in Fig. 28. Pri n, $n = 1$, 2, and 3, is the layer of primary winding. Sec n, $n = 1$ and 2, is the layer of secondary winding and Aux is auxiliary winding layer. The reason of not using a more interleaving structure: Pri1-Sec1-Pri2-Sec2-Aux-Pri3 will be explained in the following.

In the second step, the winding terminal connections should be designed to achieve the smallest CM noise based on the circuit connections in Fig. 3(a). As shown in Figs. 29 and 30, to achieve the lowest CM noise, the adjacent layers between the primary and secondary sides should have the smallest voltage difference. It is assumed that the voltage is linearly distributed along the winding, so the voltage distribution of the primary and secondary windings is shown in Fig. 30. V_{SW} is the voltage added to the primary winding. N_{P1}, N_{P2}, and N_P represent the number of turns of layer Pri1, layer Pri2, and the total number of turns of primary winding. N_S, N_{a1}, and N_{a2} are the number of turns of the secondary winding, auxiliary winding 1, and auxiliary winding 2. The y-axis is the height of the winding layers.

It is assumed that the parasitic capacitance is evenly distributed between two adjacent layers; the displacement current between two adjacent layers can be theoretically calculated [5]. For example, the total displacement current $i_{\mathrm{CM\_Pri\_Sec1}}$ between Pri1 and Sec1 is calculated by integrating the displacement current along the y-axis in (20), where C_{P_S}

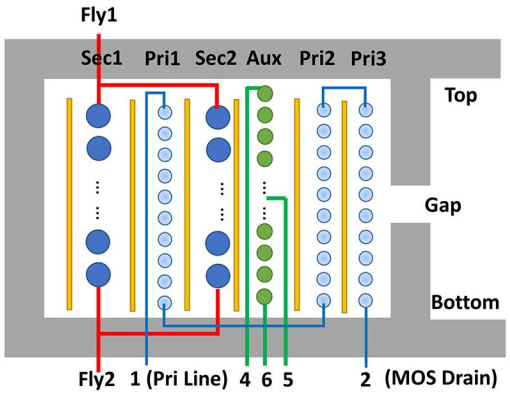

Fig. 29. Step 2: optimize winding terminal connections to reduce CM noise.

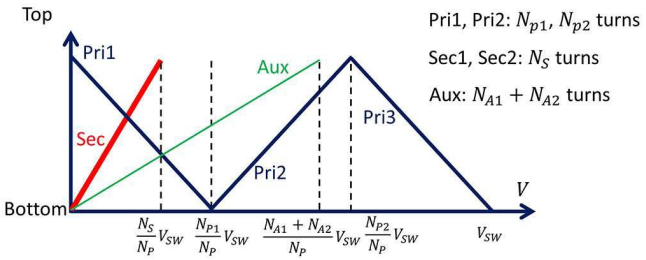

Fig. 30. Voltage distribution along windings.

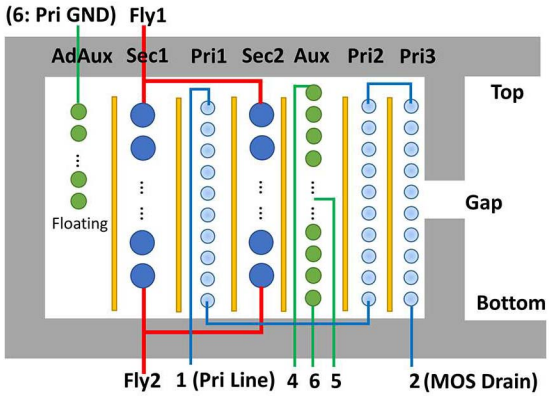

Fig. 31. Step 3: add an extra auxiliary winding AdAux to cancel CM noise.

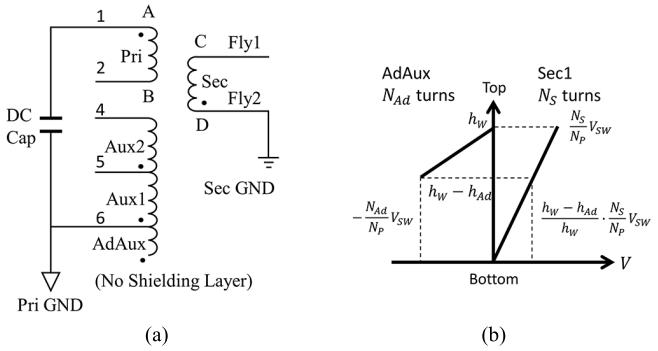

Fig. 32. AdAux winding for CM noise cancellation. (a) Transformer circuit. (b) Voltage distribution along AdAux and Sec1 windings.

is the total parasitic capacitance between the two layers and h_W is the height of the winding layer. It is obvious that the displacement current is propositional to the difference of the average voltages, $N_{\rm P1}V_{\rm SW}/(2N_P)$ and $V_SV_{\rm SW}/(2N_P)$, of the two terminal voltages across the Pri1 and Sec1 layers

$$i_{\rm CM\ Pri\_Sec1} = \int_0^{h_W} \frac{C_{P\_S}}{h_W} \cdot \frac{d}{\rm dt}\left[\left(\frac{N_{\rm P1}}{N_P}V_{\rm SW} - \frac{y}{h_W}\cdot\frac{N_{\rm P1}}{N_P}V_{\rm SW}\right) - \left(\frac{y}{h_W}\cdot\frac{N_S}{N_P}V_{\rm SW}\right)\right]{\rm dy}$$
$$= C_{P\_S}\frac{d}{\rm dt}\left(\frac{N_{\rm P1}V_{\rm SW}}{2N_P} - \frac{N_SV_{\rm SW}}{2N_P}\right). \quad (20)$$

As shown in Figs. 29 and 30, to achieve the lowest CM noise, the adjacent layers between the primary and secondary winding layers should have the lowest average voltage difference. It is shown that the net voltage difference between Pri1 and Sec1 or Sec2 is the smallest with the terminal connections shown in Fig. 29. Therefore, Pri1 is placed adjacent to two parallel secondary layers Sec1 and Sec2, as shown in Fig. 29. Similarly, Aux is placed adjacent to Sec2 layer because their voltage difference is smaller than that between Sec2 and Pri2 or Pri3. The voltage difference between Aux and Pri2 does not generate CM noise as both windings are on the primary side. On the other hand, if full interleaving winding structure Pri1-Sec1-Pri2-Sec2-Aux-Pri3 is used, the CM noise may greatly increase because of the higher voltage differences between Sec1 and Pri2, between Pri2 and Sec2, and between Sec2 and Aux layers.

In conventional techniques [2], the parasitic capacitance between two adjacent layers such as $C_{\rm P\_S}$ can be measured or calculated based on the physical winding structure. However, for multiwinding or multilayer winding structures, the accurate measurement of these capacitances is difficult, and the calculation is very complicated. It will be difficult to implement conventional technique. The parasitic capacitance extraction technique developed in Section III can solve this problem.

In the third step in Fig. 31, a cancelation auxiliary winding AdAux is added to the outer layer to cancel the CM noise. As shown in Fig. 32, when the AdAux winding starts from the top of the winding layers, the voltage difference between AdAux and Sec1 layers is the highest, which means fewer number of turns can have the same cancelation effect as more number turns when AdAux winding is located on the bottom of the layer. The number of turns, which can cancel the CM noise, of AdAux winding can be calculated based on the following process.

The displacement current $i_{\rm CM\_AdAux\_Sec1}$ from AdAux to Sec1 is given by (21), where $h_{\rm Ad}$ is the height of AdAux winding and C_{A_S} is the parasitic capacitance between Sec1 and AdAux

$$i_{\rm CM\ AdAux\_Sec1} = C_{A\_S}\cdot\frac{d}{\rm dt}\cdot\left(-\frac{N_{\rm Ad}}{2N_P}V_{\rm SW} - \frac{2h_W - h_{\rm Ad}}{2h_W}\cdot\frac{N_S}{N_P}V_{\rm SW}\right). \quad (21)$$

Under cylindrical coordinate, C_{A_S} can be calculated from (22), where r is the radius of Sec1 coil and d_w is the

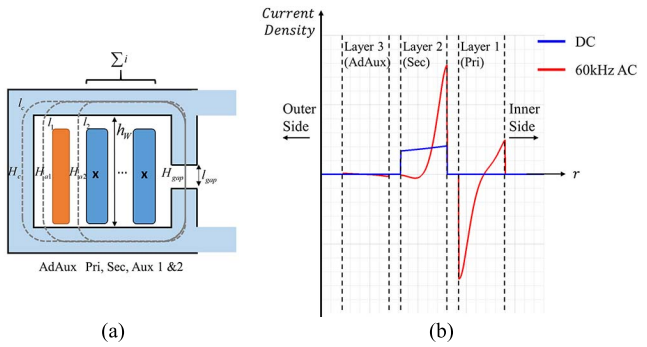

Fig. 33. Cancelation winding AdAux does not generate winding power loss because the H-field is zero. (a) H-field analysis and (b) simulated current distributions within winding layers.

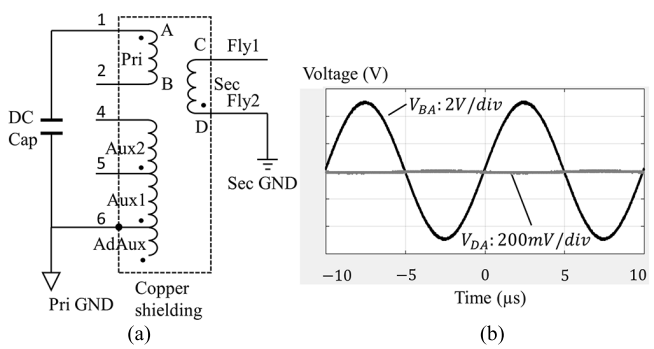

Fig. 34. Step 4: use a copper shielding to cover the core and windings to reduce CM noise. (a) Circuit and (b) balanced V_{DA} is almost equal to zero.

distance between Sec1 and AdAux layers. Equation (22) is valid based on two assumptions: 1) the fringing capacitance between two layers can be ignored and 2) r is much larger than d_w. Besides, h_{Ad} can be obtained from (23), where D_{Ad} is the distance of two adjacent turns of the AdAux winding. By substituting (22) and (23) into (20), N_{Ad} becomes the only unknown

$$C_{A\_S} \approx \frac{2\pi\varepsilon h_{\mathrm{Ad}}}{\ln(r+d_w)-\ln r} \approx 2\pi\varepsilon h_{\mathrm{Ad}} \cdot \frac{r}{d_w} \tag{22}$$

$$h_{\mathrm{Ad}} = N_{\mathrm{Ad}} \cdot D_{\mathrm{Ad}}. \tag{23}$$

Based on the two-capacitance model of the transformer as shown in Fig. 7(c), the original displacement current $i_{\mathrm{CM\_Origin}}$ before adding the AdAux winding is given in (24), where C_{BD} can be directly measured. If the sum of $i_{\mathrm{CM\_AdAux\_Sec1}}$ and $i_{\mathrm{CM\_Origin}}$ equals to zero, the transformer achieves CM balance. Therefore, N_{Ad} can be directly solved in (25). Based on the technique introduced in Section III, the balance can be examined with a signal generator and an oscilloscope

$$i_{\mathrm{CM\ Origin}} = C_{\mathrm{BD}} \frac{\mathrm{dV_{SW}}}{\mathrm{dt}} \tag{24}$$

$$N_{\mathrm{Ad}} = \frac{\sqrt{N_S^2 h_W^2 + N_P h_W \cdot (h_W - D_{\mathrm{Ad}} \cdot N_S) \cdot \frac{C_{\mathrm{BD}} d_w}{\pi \varepsilon r D_{\mathrm{Ad}}}} - N_S h_W}{h_W - D_{\mathrm{Ad}} \cdot N_S}. \tag{25}$$

In the analysis above, the auxiliary winding AdAux is located at the outer layer of the windings so it is convenient to adjust N_{AD}. In Fig. 33(a), the H-field is analyzed for one winding window of the transformer. As shown in Fig. 33(a), because the transformer core has a much higher permeability than the air gap l_{gap} in the center leg, the H-field H_{gap} in the air gap is much higher than that of the H-field H_c, which is almost zero, inside the core. h_W is the height of the winding layer. Based on Ampere's law in (26), $H_{\mathrm{gap}} l_{\mathrm{gap}}$ is almost equal to the total magnetic motive force $\sum i$ generated by transformer windings. When the AdAux winding is at the outer layer of the winding, based on Ampere's law in (27) and (28), the H-field H_{a1} and H_{a2} on the surfaces of AdAux winding is zero because $H_{\mathrm{gap}} l_{\mathrm{gap}} = \sum i$. Because of this, there is almost no power loss due to the eddy currents induced by the H-field in the AdAux winding. Fig. 33(b) shows the simulated current distributions within winding layers at 60-kHz switching frequency. It is shown that the AdAux layer has almost zero-induced currents as predicted

$$\sum i = \oint_{l_c} \mathrm{Hdl} = H_c l_c + H_{\mathrm{gap}} l_{\mathrm{gap}} \approx H_{\mathrm{gap}} l_{\mathrm{gap}} \tag{26}$$

$$\sum i = \oint_{l_1} \mathrm{Hdl} \approx h_W H_{a1} + H_{\mathrm{gap}} l_{\mathrm{gap}} \Rightarrow H_{a1} = 0 \tag{27}$$

$$\sum i = \oint_{l_2} \mathrm{Hdl} \approx h_W H_{a2} + H_{\mathrm{gap}} l_{\mathrm{gap}} \Rightarrow H_{a2} = 0. \tag{28}$$

On the other hand, if the AdAux winding is located between other winding layers, the H-field will not be zero; eddy current power loss will be induced in AdAux winding. The conventional shielding layers in Fig. 3(b) have eddy current power loss too because the H-field on the shielding layers is not zero.

Similarly, the power loss of core copper shielding introduced in Fig. 24 can also be analyzed. When the airgap is at center leg of the core, the H-field outside the transformer windings is very small; thus, there is no power loss in the core copper shielding.

The last step is to apply a copper shielding to transformer core to eliminate the capacitive couplings due to the core. The copper shielding is tied to terminal 6, Pri GND, of the transformer as shown in Fig. 34(a). Based on previous analysis in Section IV, using a copper shielding to cover the core will slightly change the CM balance of the transformer because the secondary winding in Fig. 31 is not fully in the middle of the windings. So, the number of turns of AdAux winding should be slightly adjusted with a signal generator and an oscilloscope in the last step to achieve a new balance. The measured V_{DA} after the fourth step is almost equal to zero, as shown in Fig. 34(b). A good CM noise balance is achieved.

Using the AdAux winding at outer winding layer can also reduce the leakage inductance of the transformer. The leakage inductance of transformers is equivalently determined by the magnetic energy stored in the space between winding layers [21]. In a 2-D system, as shown in Fig. 31, the magnetic energy stored in the space between winding layers is equal to the magnetic energy density $\mu H^2/2$ times the space volume $h_W d_W$, where d_W is the distance between two-winding layers.

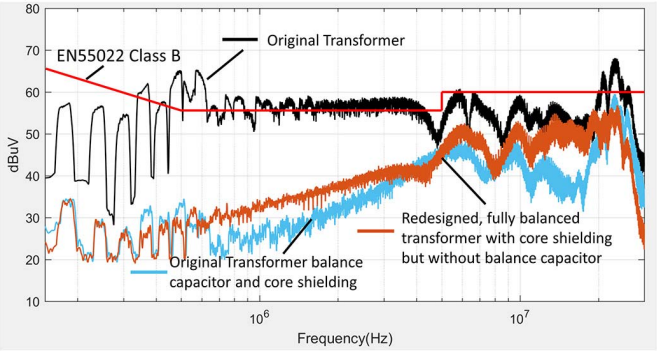

Fig. 35. Comparison of the measured CM noise.

Based on Ampere's law, the H-field in the space between two winding layers is determined by the winding currents, so it is independent of space volume. The magnetic energy stored in the space between two winding layers is, therefore, proportional to the distance between two winding layers. Because adding a shielding layer between two winding layers as shown in Fig. 3(b) can increase the distance between two winding layers, the magnetic energy stored in the space between two winding layers, and therefore the leakage inductance will increase. The AdAux winding will not increase the space between winding layers, so the transformer has smaller leakage inductance than that of the transformer with conventional shielding layers in Fig. 3(b).

The advantages of the proposed design steps above are summarized in the following.

1) Since the voltage on the AdAux winding can be negative and it grows rapidly as the number of turns increases, the balance capability of the adjustable auxiliary winding is better than conventional shielding layers which can only shield two adjacent layers.
2) Although the proposed technique adds one AdAux layer, it removes two shielding layers. Therefore, it simplifies transformer winding structure and achieves both the size and cost reduction for the transformer.
3) Because there are no shielding layers between winding layers, the mutual coupling between windings is higher than that with shielding layers; this leads to smaller leakage inductance.
4) Since there is no eddy current power loss in AdAux winding, the ac winding loss of the transformer is smaller than that with shielding layers between the primary and secondary winding layers.
5) Because no balance capacitor is used, there is no safety issue introduced by the capacitor and there is no extra 50-/60-Hz leakage current between primary and secondary too.

Most importantly, with the help of the transformer balance measurement technique proposed in Section III, the AdAux winding layer can be designed quickly and conveniently without any in-circuit tests.

C. Experimental Verification

To verify the proposed transformer design technique, a prototype was developed in Fig. 34(a) based on the proposed design steps above. The designed parameters are shown in Table I. Auxiliary winding turn N_{Ad} is calculated as around 15.5. A transformer is made and its CM performance is examined based on the technique developed in Section III. The CM performance of the transformer is the best after adjusting AdAux winding number to 14, when V_{DA} is close to zero as shown in Fig. 34(b). CM noise is well balanced inside the transformer windings. The transformer was used in a commercial Flyback converter for CM noise measurement after its CM EMI filter and Y-capacitor were removed. The measured CM noise is shown in Fig. 35 and compared with the measured noise with the original commercial transformer, and with the original commercial transformer having core copper shielding and the balance capacitor.

TABLE I
PARAMETERS USED IN ADAUX WINDING DESIGN

Parameter	Quantity	Parameter	Quantity
$h_W(mm)$	10.63	$C_{BD}(pF)$	10.5
$D_{Ad}(mm)$	0.25	N_S	8
$d_w(mm)$	0.14	N_P	40
$r(mm)$	9.5	N_{Ad}	15.5

The CM noise of the original commercial adapter exceeds EMI standard EN55022 class B from 500 kHz if its CM filter and Y-Cap were removed. After adding a balance capacitor and a core shielding, the CM noise is reduced by up to 35 dB at low frequencies. However, at 22 MHz, the CM noise still cannot fully meet the standard. With the redesigned transformer based on the proposed steps above, the CM noise meets the EMI standard in whole frequency range with 4–30-dB margin.

The leakage inductance between the primary and other windings of the transformers is measured using an impedance analyzer. In the measurement, the leakage inductance of the primary winding is measured with all other windings shorted. Compared with the original transformer with conventional shielding layers in Fig. 3, the measured leakage inductance of the redesigned transformer is reduced from 6 to 5 μH. (The magnetizing inductance of the Flyback transformer is 630 μH.)

Because no Y-capacitors or balance capacitors are used across primary and secondary sides with the redesigned transformer, there is no safety issue too. With the redesigned transformer, the original CM EMI filter and Y-cap have been successfully removed from the power adapter.

VI. CONCLUSION

This paper first developed a two-capacitance transformer winding capacitance model for a multiwinding Flyback transformer without investigating complicated transformer winding structures. A measurement technique using a signal generator and an oscilloscope to extract parasitic capacitance and evaluate the CM noise performance of a transformer was proposed. The technique is very convenient for mass testing because no in-circuit tests are needed. This has been verified by transformer manufacturers. The near electric field coupling due to transformer cores was investigated and the core shielding

technique is investigated to reduce this coupling. Balance capacitor and winding design techniques are investigated based on the developed two-capacitance model to achieve small CM noise and small leakage inductance. Experiments verified all of the proposed techniques. The CM noise of the Flyback adapter prototype can meet the EMI standards without using CM EMI filters and Y-capacitors.

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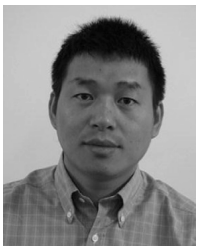

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